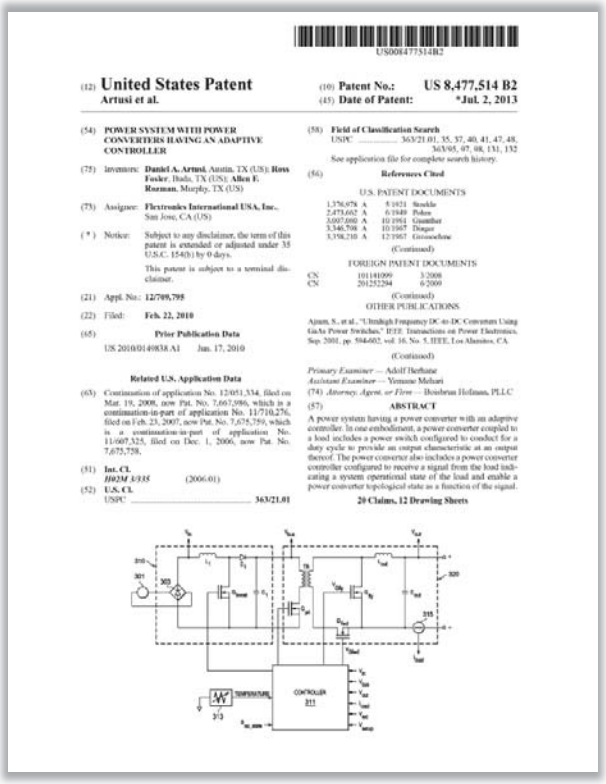
EXHIBIT H

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800, EP-TA845, S2MM101



US008477514B2

(12) **United States Patent**
Artusi et al.

(10) **Patent No.: US 8,477,514 B2**
(45) **Date of Patent: *Jul. 2, 2013**

(54) **POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER**

(75) Inventors: **Daniel A. Artusi**, Austin, TX (US); **Ross Fosler**, Buda, TX (US); **Allen F. Rozman**, Murphy, TX (US)

(73) Assignee: **Flextronics International USA, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/709,795**

(22) Filed: **Feb. 22, 2010**

(65) **Prior Publication Data**

US 2010/0149838 A1 Jun. 17, 2010

Related U.S. Application Data

(63) Continuation of application No. 12/051,334, filed on Mar. 19, 2008, now Pat. No. 7,667,986, which is a continuation-in-part of application No. 11/710,276, filed on Feb. 23, 2007, now Pat. No. 7,675,759, which is a continuation-in-part of application No. 11/607,325, filed on Dec. 1, 2006, now Pat. No. 7,672,758.

(51) **Int. Cl.**
H02M 3/335 (2006.01)

(52) **U.S. Cl.**
USPC **363/21.01**

(58) **Field of Classification Search**
USPC 363/21.01, 35, 37, 40, 41, 47, 48, 363/95, 97, 98, 131, 132
See application file for complete search history.

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Assistant Examiner — Yemane Mehari
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(57) **ABSTRACT**

A power system having a power converter with an adaptive controller. In one embodiment, a power converter coupled to a load includes a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof. The power converter also includes a power converter controller configured to receive a signal from the load indicating a system operational state of the load and enable a power converter topological state as a function of the signal.

20 Claims, 12 Drawing Sheets

Title: POWER SYSTEM WITH POWER CON VERTERS HAVING AN ADAPTIVE CONTROLLER

Priority Date: Dec. 01, 2006

Filed Date: Feb. 22, 2010

Issued Date: Jul. 02, 2013

Expiration Date: Dec. 01, 2026

Inventors: Daniel A. Artusi; Ross Fosler; Allen F. Rozman

Claims: 1, 5, & 16

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

Claim 1

A **(CON) power converter** coupled to a **(LD) load**, comprising:

a **(PS) power switch configured to conduct for** a **(DC) duty cycle** to provide an **(OC) output characteristic** at an **(OUT) output**; and

a **(PCC) power converter controller configured to receive** a **(S) signal** from said **(LD) load** indicating a **(OP) system operational state** of said **(LD) load** and

control an **(IOC) internal operating characteristic** of said **(CON) power converter** as a function of said **(S) signal**.

Claim 5

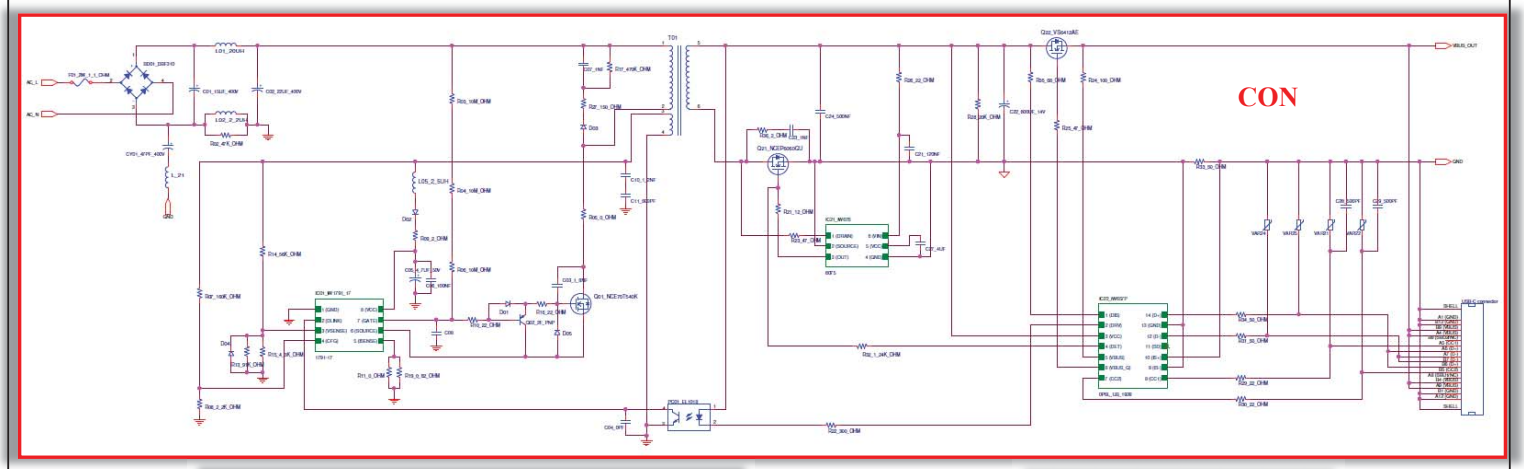
The **(CON) power converter** as recited in claim 1 wherein said **(IOC) internal operating characteristic** is selected from the group consisting of:

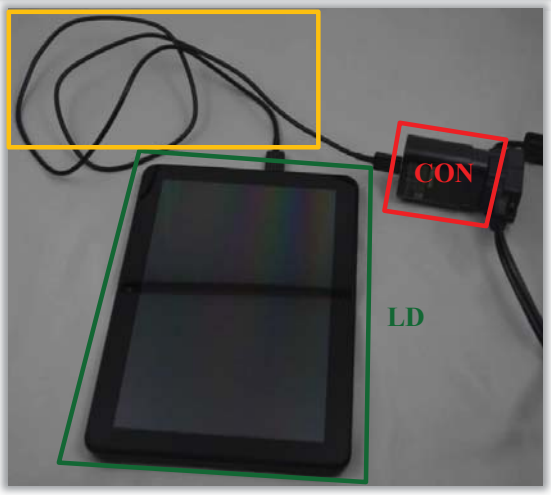
a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an **(VBUS) internal direct current bus voltage** of said **(CON) power converter**.

Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

A **(CON) power converter** **coupled to** a **(LD) load**, comprising:

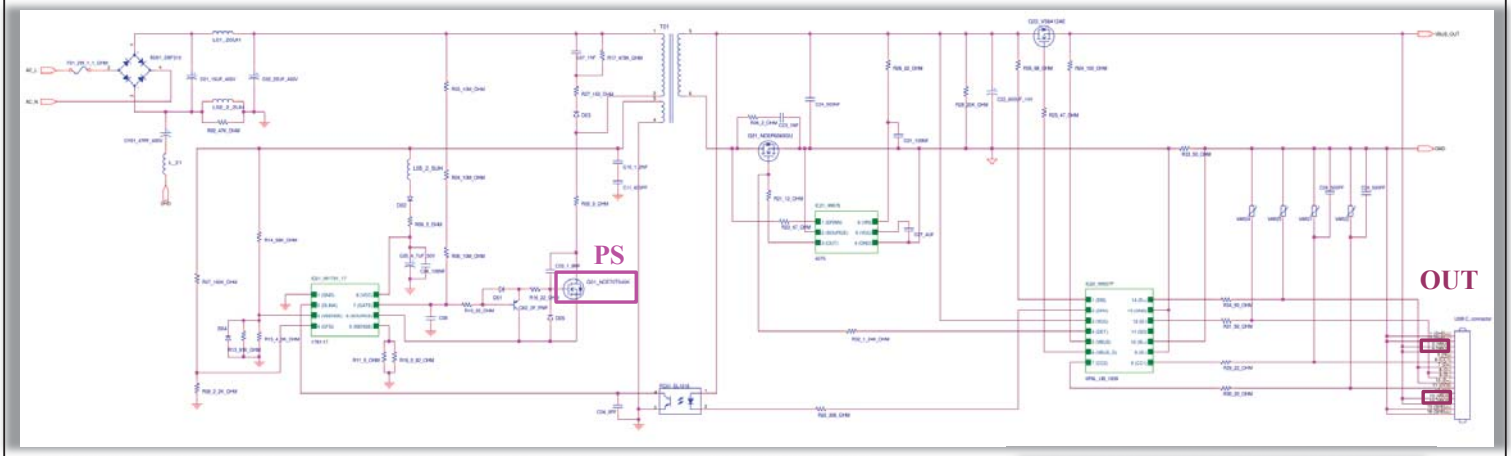




Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

a **(PS) power switch configured to conduct for** a duty cycle to provide an **(OC) output characteristic** at an **(OUT) output**; and

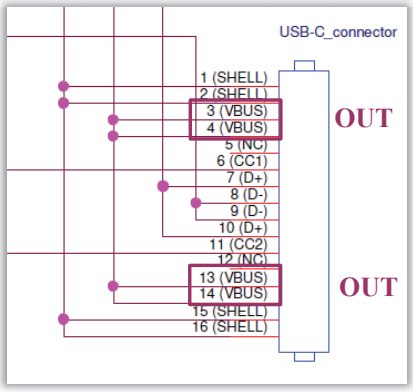


4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports **OC**
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*

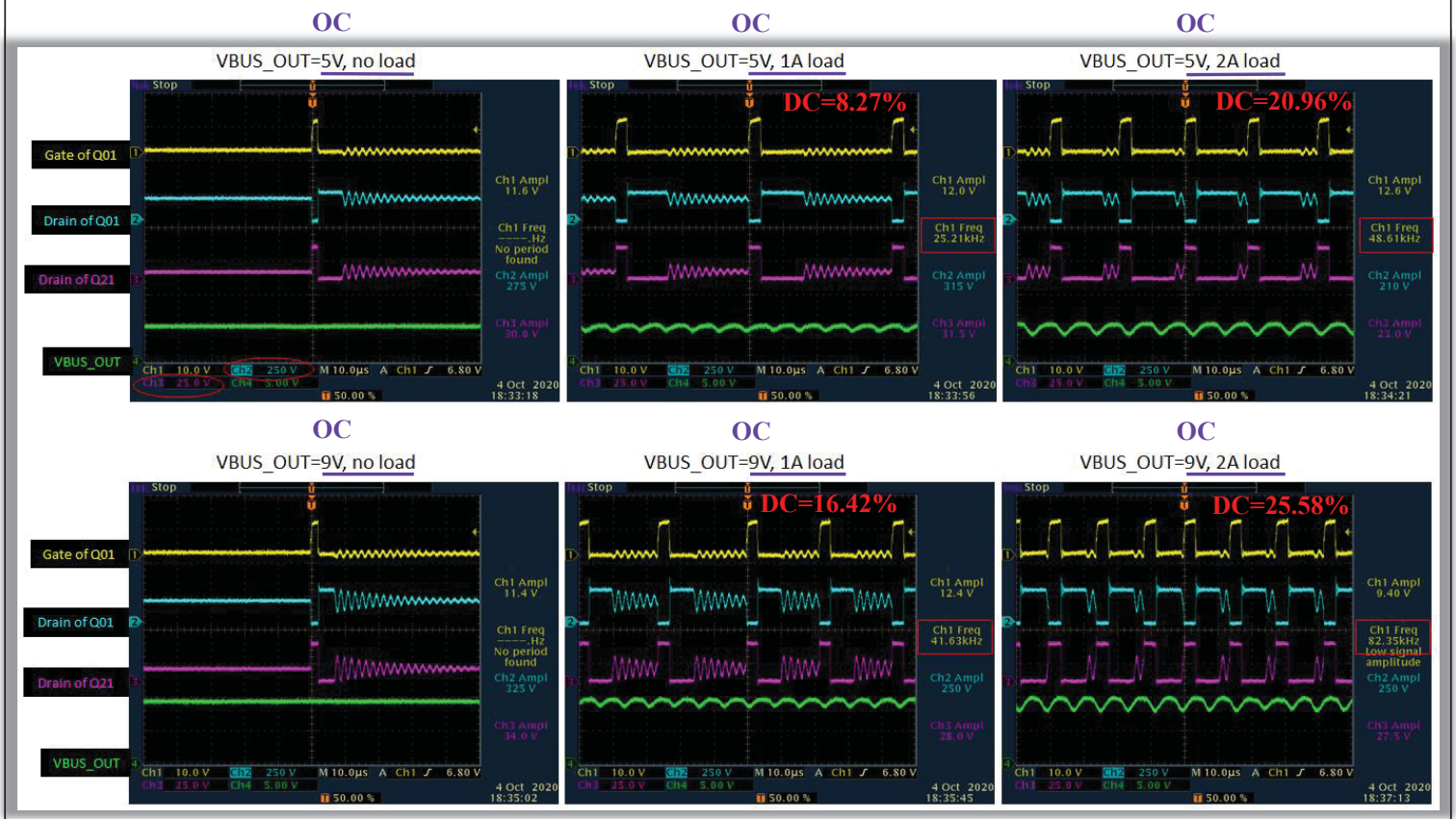


Source: https://usb.org/sites/default/files/USB%20Type-C%20Spec%20R2.0%20-%20August%202019.pdf, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

a power switch configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an output; and



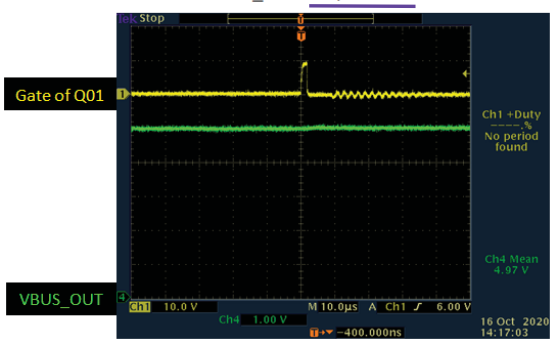
Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

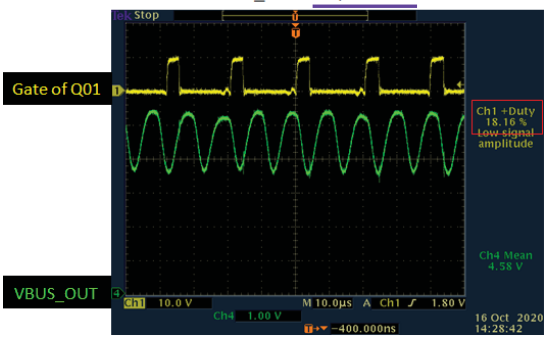
a power switch configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an output; and

OC

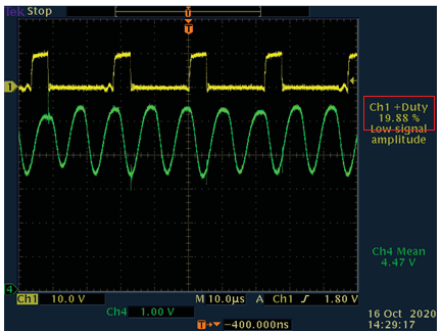
VBUS_OUT= 5V, no load



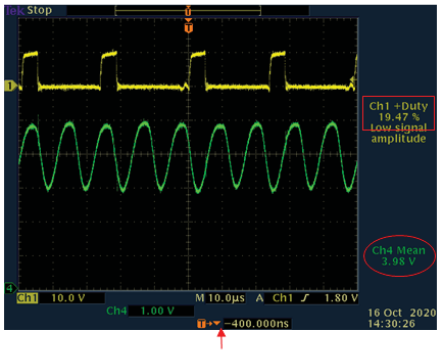
VBUS_OUT= 5V, 3A load **OC**



VBUS_OUT= 5V, 3.5A load **OC**



VBUS_OUT= 5V, ~3.6A load **OC**

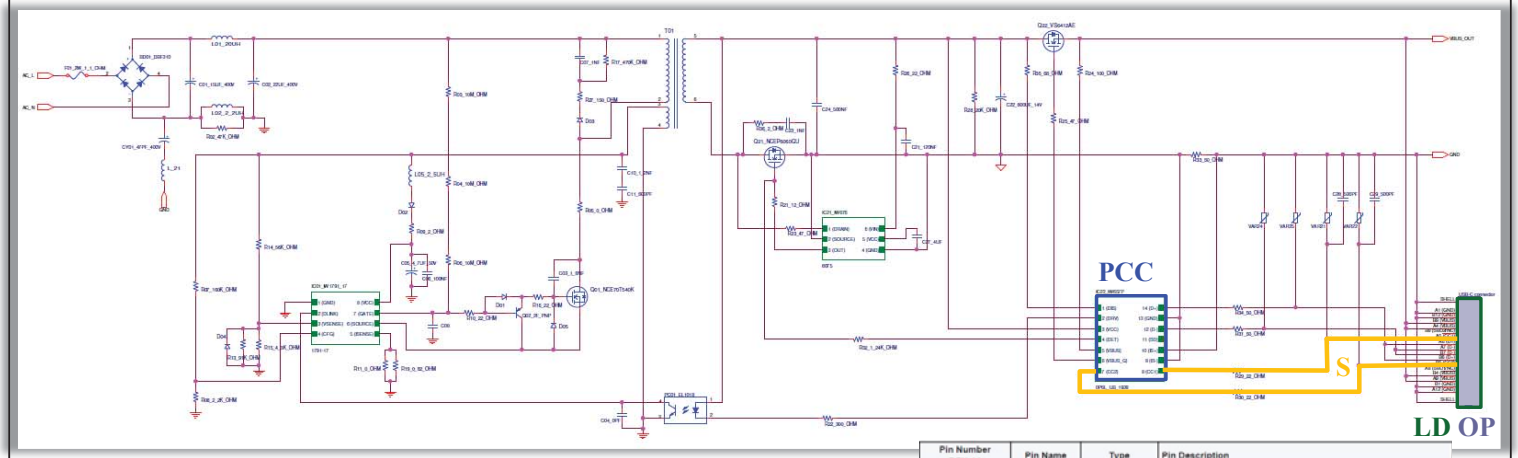


Note: The charger will hold up the VBUS_OUT voltage at ~4.5V under a 3.5A load but the charger shuts down when the load is increased beyond that. This O-scope capture was taken as the charger was going into one of those over-current protection shutdowns when the load was increased to ~3.6A. Immediately after this capture, the VBUS_OUT voltage drops to 0V.

Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

a **(PCC) power converter controller configured to receive** a **(S) signal** from said **(LD) load** indicating a **(OP) system operational state** of said **(LD) load** and



IC22 works in conjunction with IC21 and IC01.

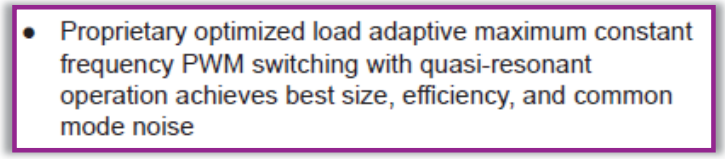
Pin Number DFN-14	Pin Name	Type	Pin Description
1	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
2	DRV	Analog Output	External circuit drive. Can be used to drive optocoupler LED with automatic current limiting for transmitting signals to primary side.
3	V_{CC}	Power Supply	IC power supply.
4	DET	Analog Input	AC unplug detect.
5	V_{BUS}	Analog Input/ Output	Monitor V_{BUS} voltage after N-FET switch.
6	V_{BUS_G}	Analog Input/ Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/ Output	Configuration Channel 2. S
8	CC1	Analog Input/ Output	Configuration Channel 1.
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).
11	SD	Analog Input/ Output	Connect to an external NTC resistor to measure the power adapter temperature.
12	D-	Analog Input/ Output	USB D- signal.
13	GND	Ground	Ground.
14	D+	Analog Input/ Output	USB D+ signal.

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0 30-Mar-2020, Note: The citation pertains to only the document excerpt not the schematics or other data.

control an **(IOC) internal operating characteristic** of said **(CON) power converter** as a function of said signal.

CON

IOC

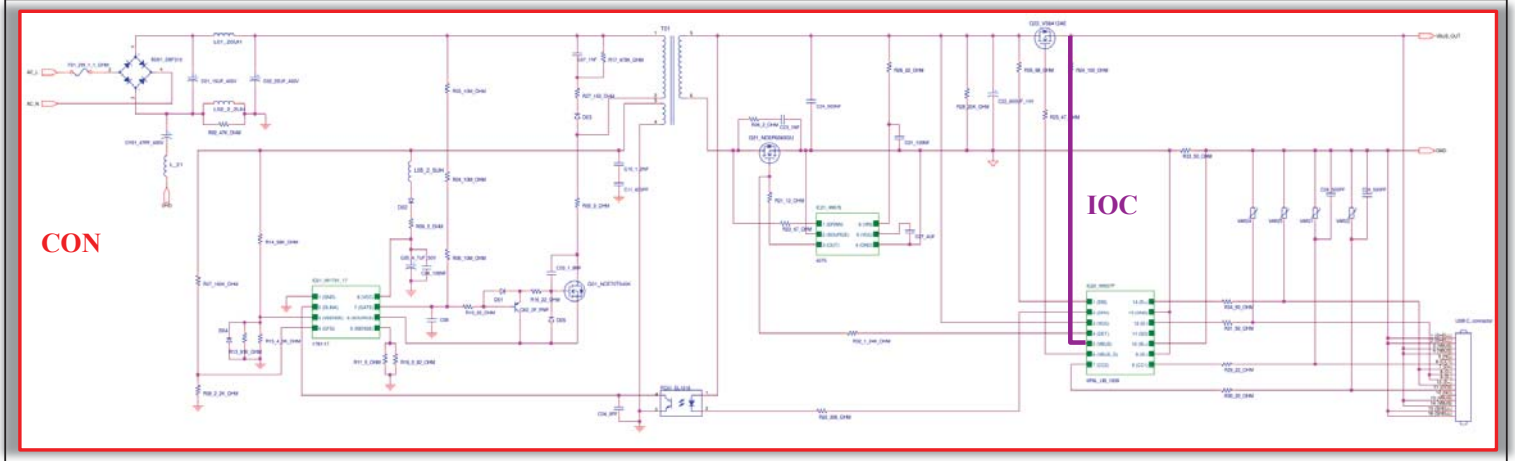


Source: Dialog Semiconductor iW1791 AC/DC Primary Side Rapid Charge PWM Controller with High Resolution Voltage/Current Control, Product Summary Rev. 1.51 05-OCT-2018

Claim 5

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

The **(CON) power converter** as recited in claim 1 wherein said **(IOC) internal operating characteristic** is selected from the group consisting of:



IOC

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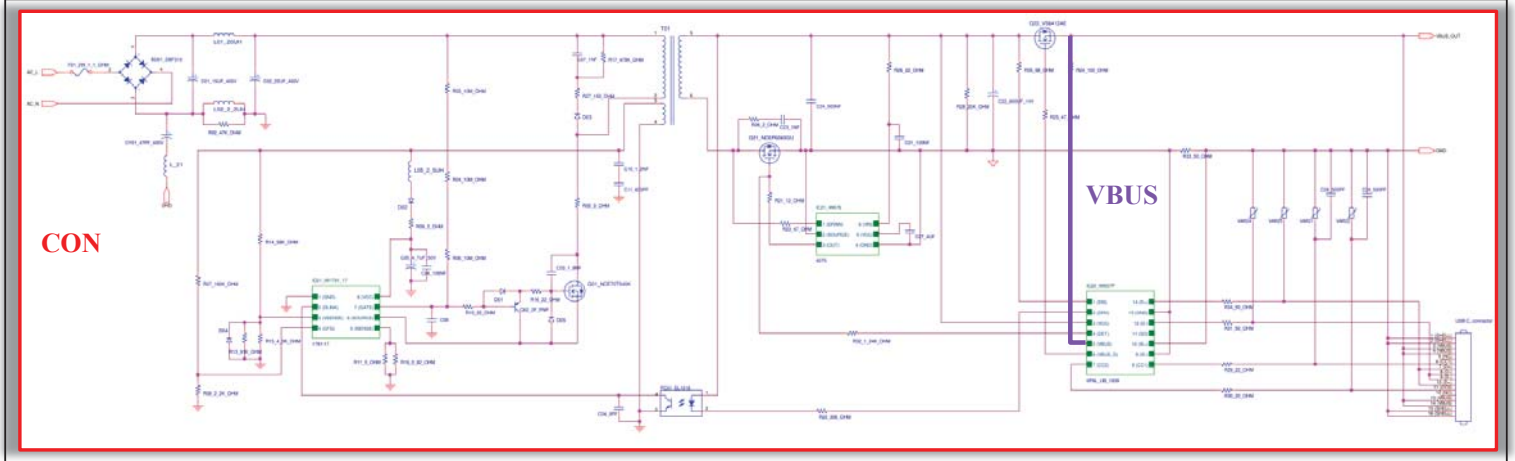
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0

Claim 5

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA800

a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an **(VBUS) internal direct current bus voltage** of said **(CON) power converter**.



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4	DET	Analog Input	AC unplug detect.
5	V_{BUS}	Analog Input/ Output	Monitor V_{BUS} voltage after N-FET switch. **VBUS**
6	V_{BUS_G}	Analog Input/ Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/ Output	Configuration Channel 2.
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9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).

Source: Dialog Semiconductor iW657P USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+, Product Summary Rev. 1.0

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA845

Claim 1

A **(CON) power converter** coupled to a **(LD) load**, comprising:

a **(PS) power switch configured to conduct for** a **(DC) duty cycle** to provide an **(OC) output characteristic** at an **(OUT) output**; and

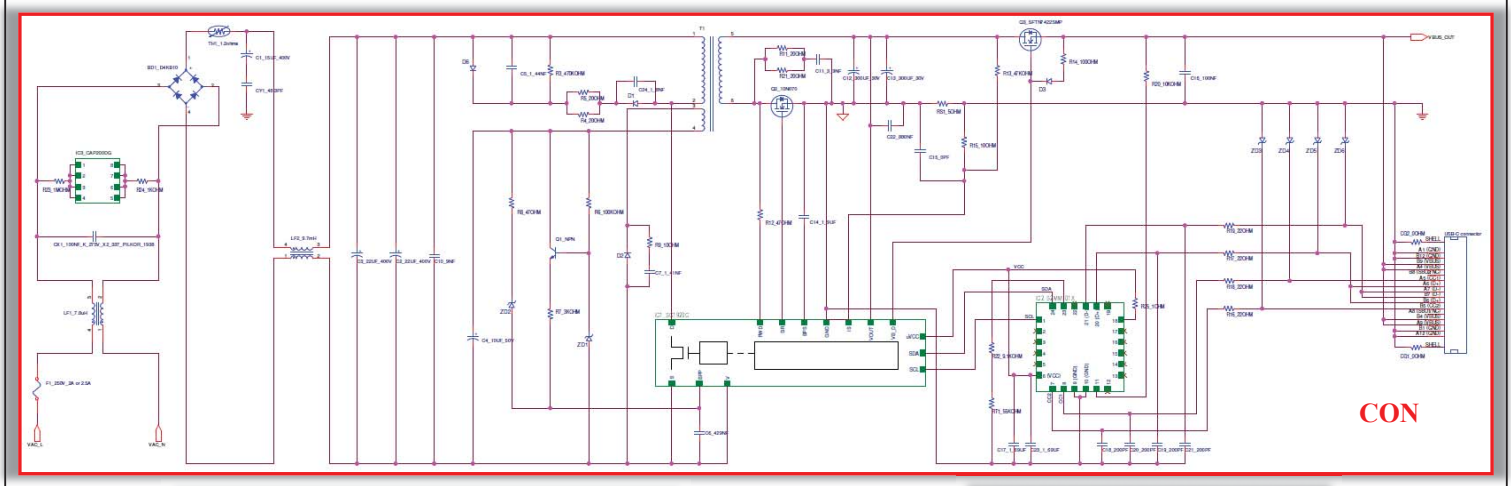
a **(PCC) power converter controller configured to receive** a **(S) signal** from said **(LD) load** indicating a **(OP) system operational state** of said **(LD) load** and

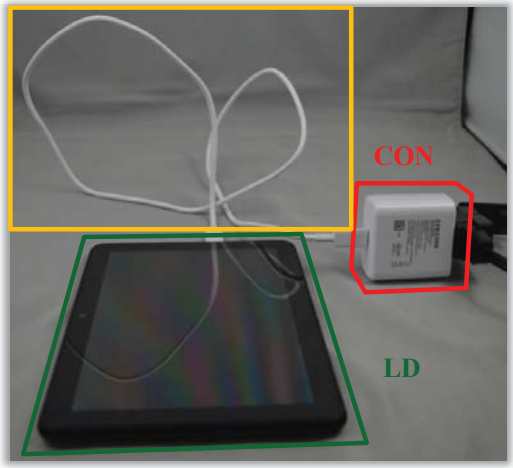
control an **(IOC) internal operating characteristic** of said **(CON) power converter** as a function of said **(S) signal**.

Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA845

A **(CON) power converter** coupled to a **(LD) load**, comprising:

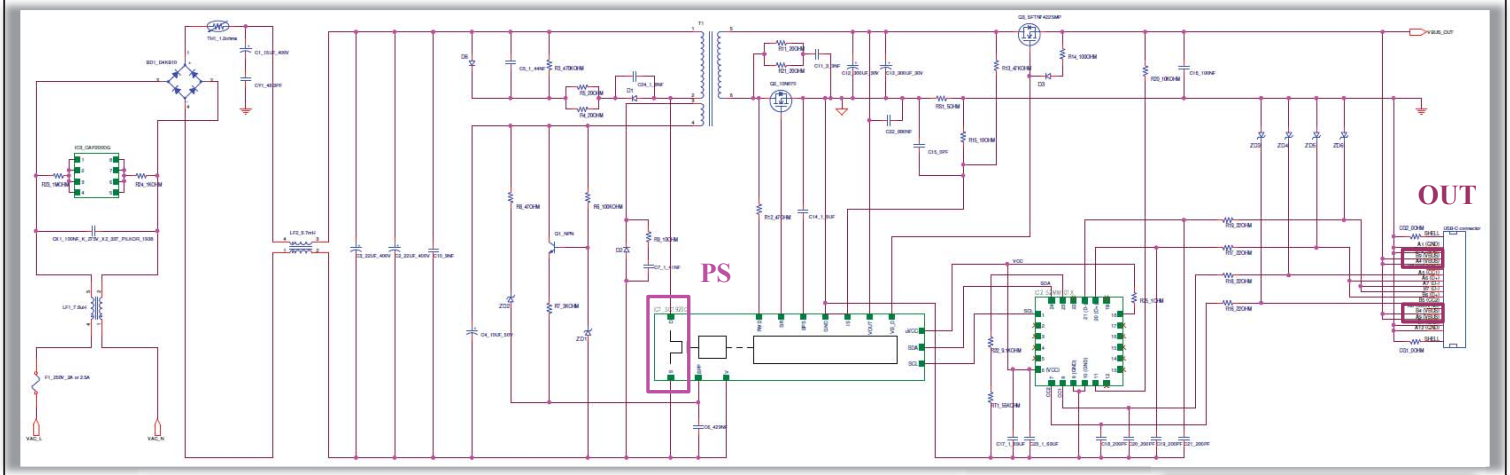




Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA845

a **(PS) power switch configured to conduct for** a duty cycle to provide an **(OC) output characteristic** at an **(OUT) output**; and



4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
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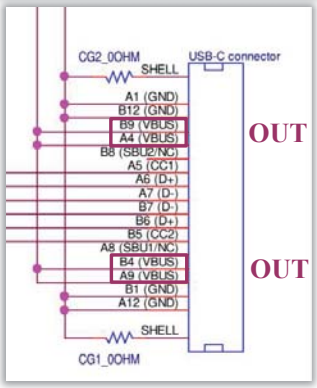
- Establish data roles between two attached ports **OC**
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*

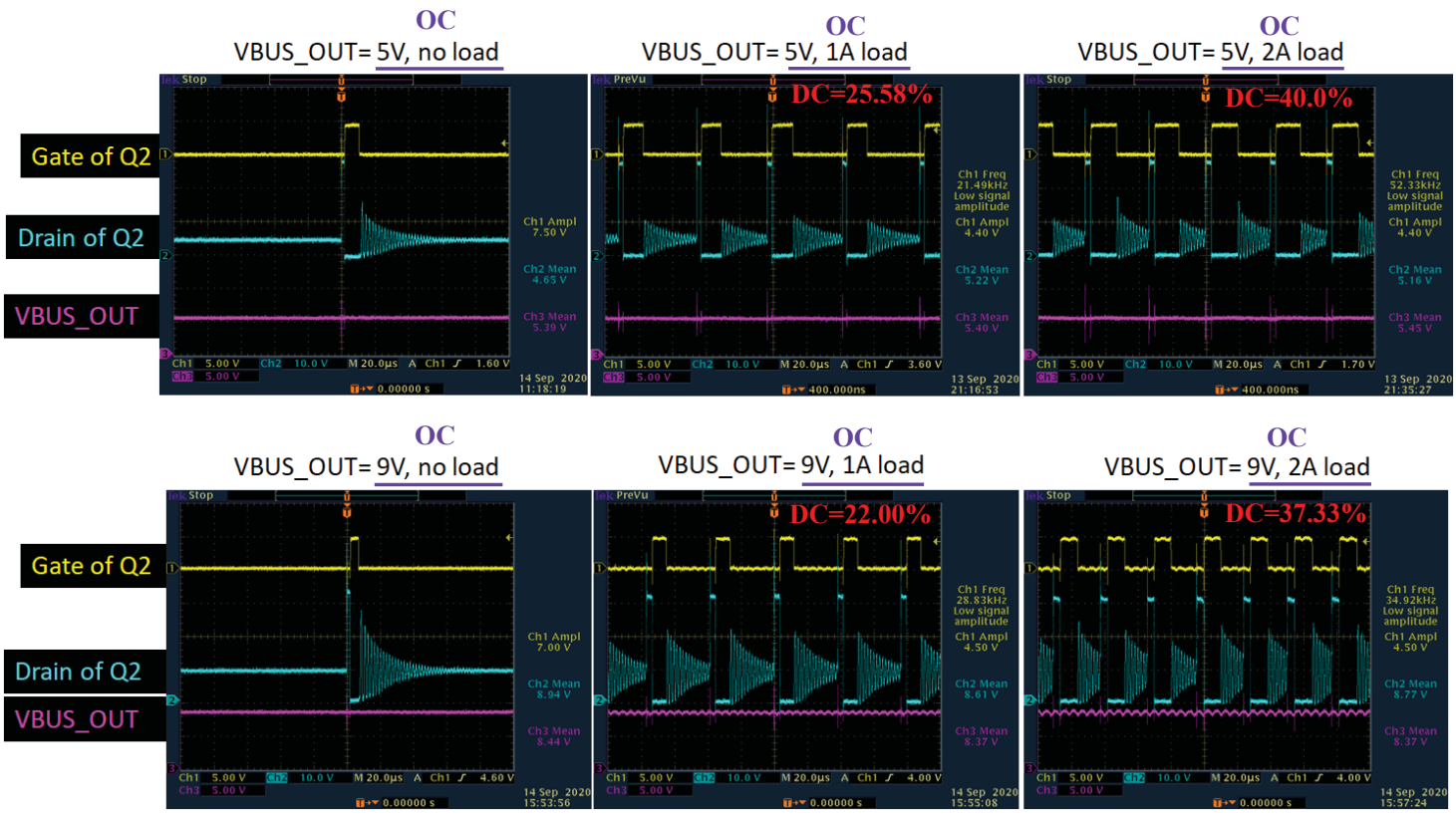


Source: https://usb.org/sites/default/files/USB%20Type-C%20Spec%20R2.0%20-%20August%202019.pdf, Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA845

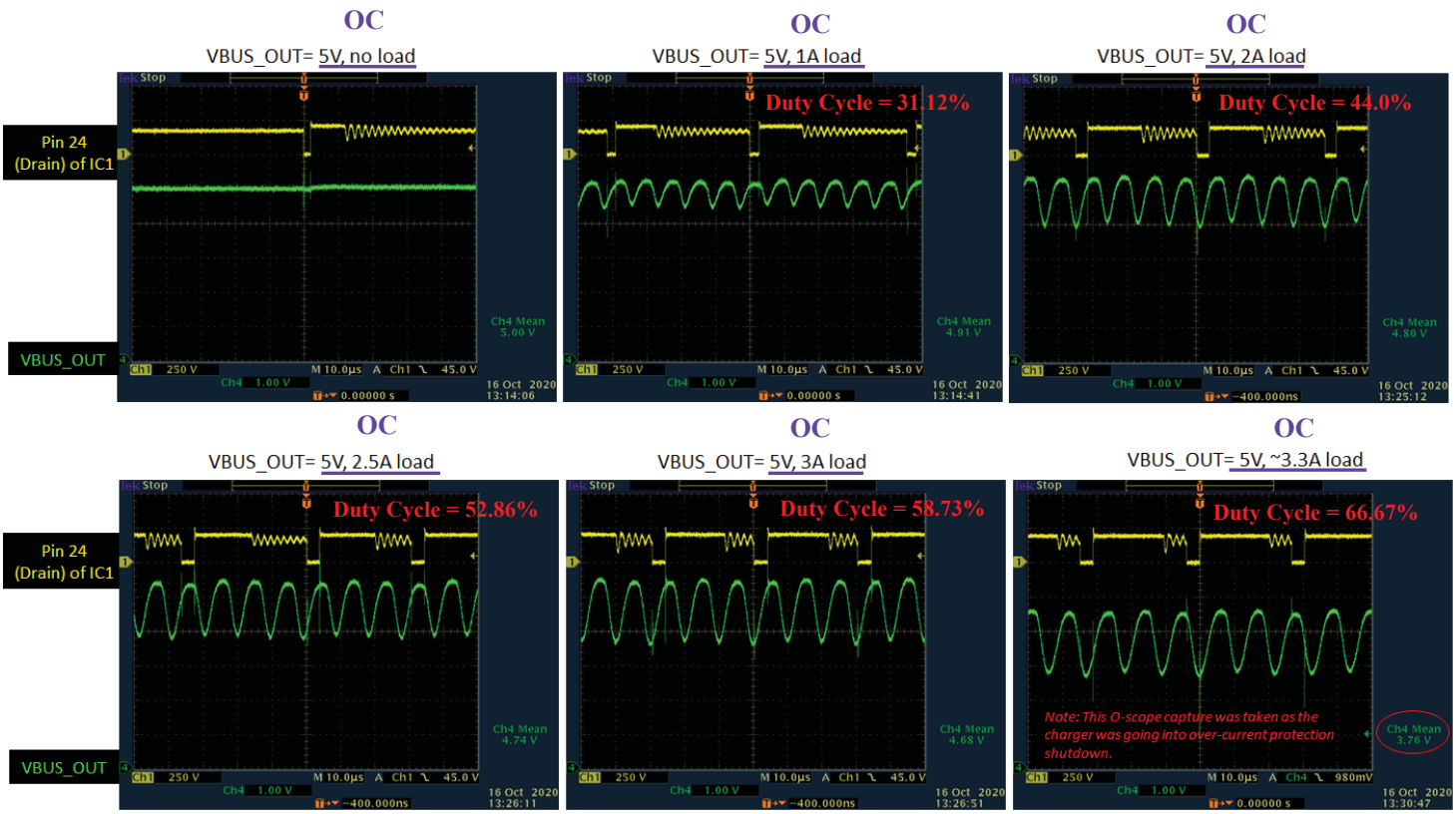
a power switch configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at output; and



Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA845

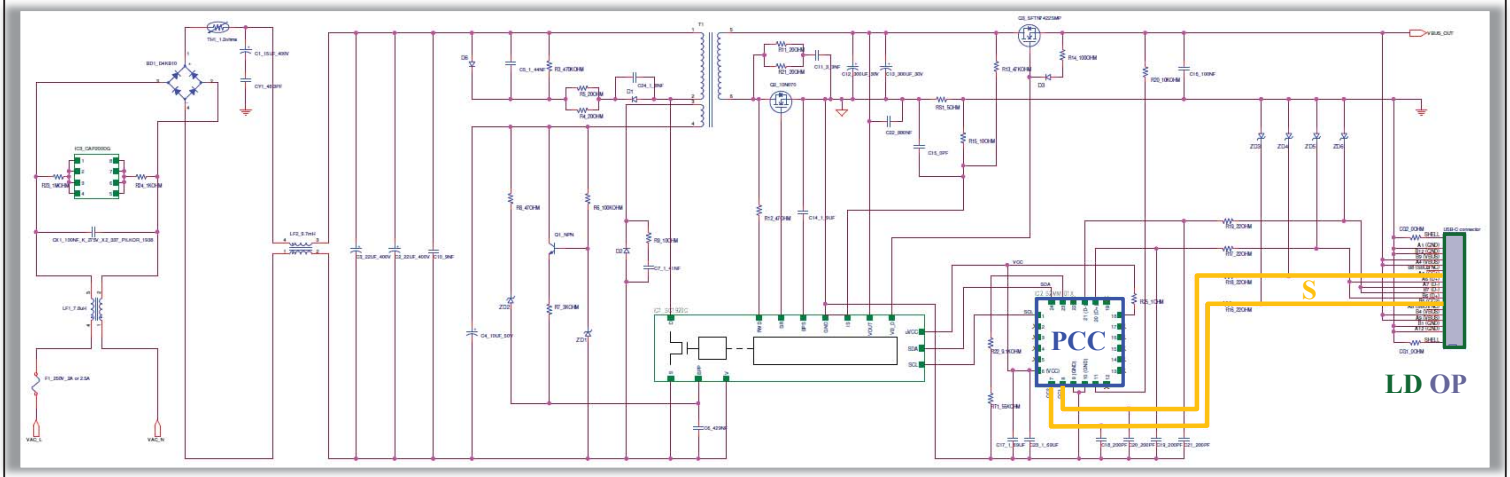
a power switch configured to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an output; and



Claim 1

Exhibit H - U.S. Patent No. 8,477,514 – Samsung EP-TA845

a **(PCC) power converter controller configured to receive** a **(S) signal** from said **(LD) load** indicating a **(OP) system operational state** of said **(LD) load** and



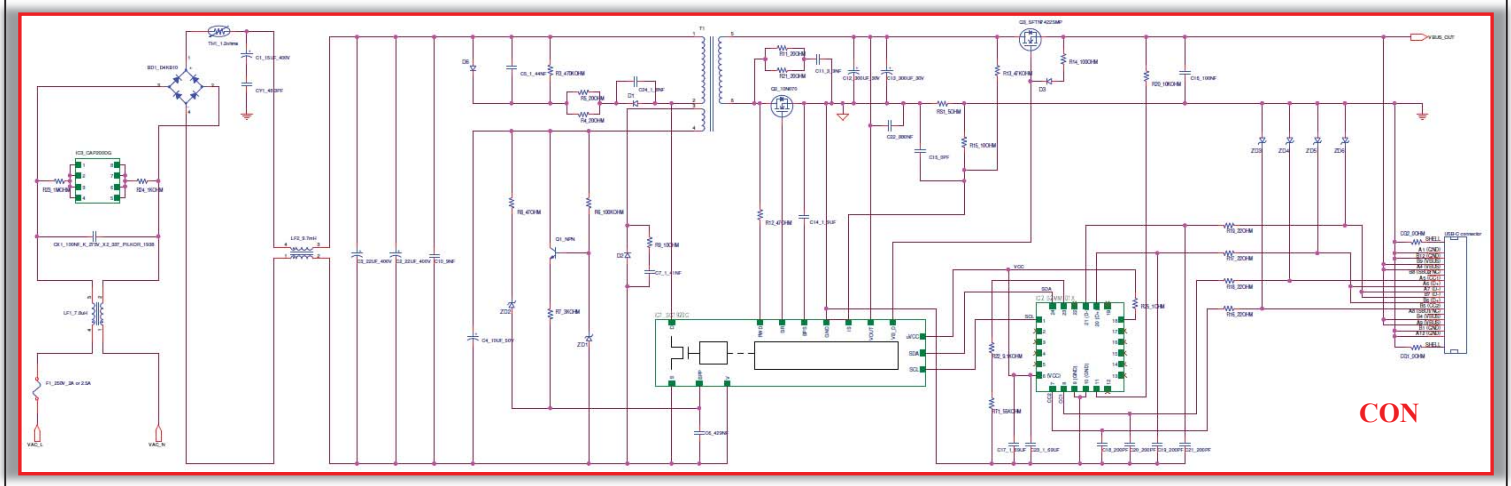
OP

Highly Integrated, Compact Footprint

- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.

control an **(IOC) internal operating characteristic** of said **(CON) power converter** as a function of said signal.



IOC

Highly Integrated, Compact Footprint

- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

Source: InnoSwitch3-Pro Family, Rev. M 8/20, Note: The citation pertains to only the document excerpt not the schematics or other data.

Exhibit H - U.S. Patent No. 8,477,514 – Samsung S2MM101

Claim 16

A method of operating a **(SYS) power system**, comprising:

enabling operation of components of a **(PRO) processor system** to establish a **(DRN) state of power drain** thereof;

providing a **(S) signal to identify operation** of said **(PRO) processor system** in said **(DRN) state of power drain**;

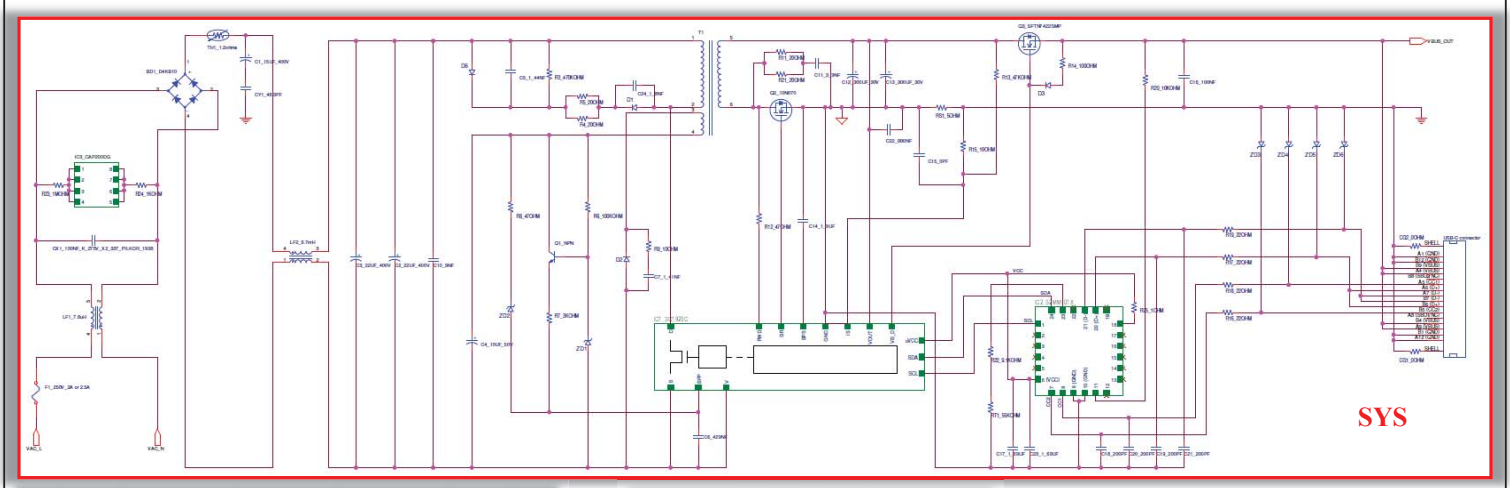
sensing a **(PL) power level of said state of power drain** in response to said **(S) signal**; and

controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.

Claim 16

Exhibit H - U.S. Patent No. 8,477,514 – Samsung S2MM101

A method of operating a **(SYS) power system**, comprising:



Claim 16

Exhibit H - U.S. Patent No. 8,477,514 – Samsung S2MM101

enabling operation of components of a **(PRO) processor system** to establish a **(DRN) state of power drain** thereof;

PRO

4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.

Table 4-14 Source Port CC Pin State

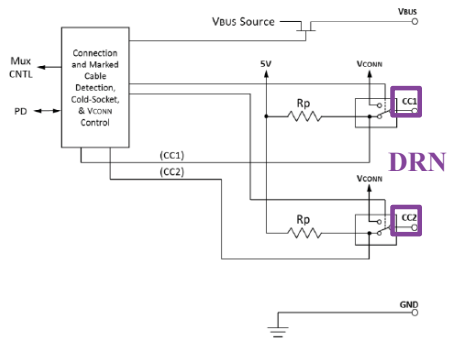
CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	Open, Rp	Above vOPEN
SRC.Rd	Rd	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	Ra	Below maximum vRa

Table 4-15 Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	Rp	Above minimum vRd-Connect
SNK.Open	Open, Ra, Rd	Below maximum vRa

Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.

Figure 4-7 Source Functional Model for CC1 and CC2



Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN.
5. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

The source functional model detects CC1/CC2 and dynamically adjusts the current, voltage x current is the state of power drain.

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16

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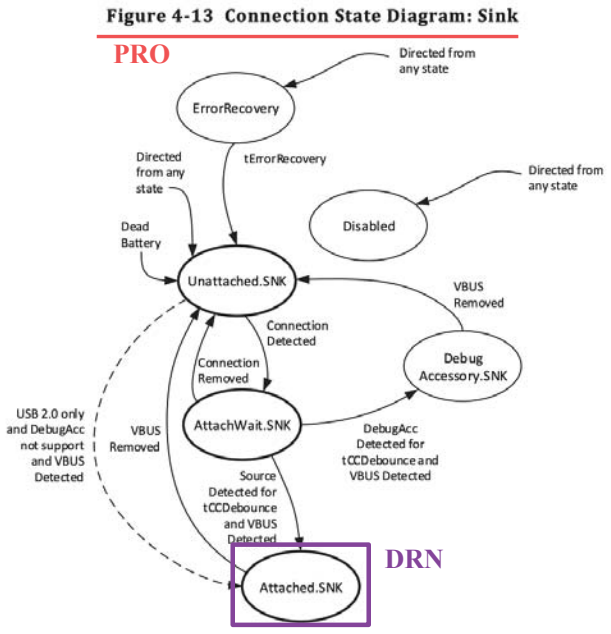
enabling operation of components of a **(PRO) processor system** to establish a **(DRN) state of power drain** thereof;

Figure 4-13 illustrates a connection state diagram for a simple Sink (Device/Hub UFP).

Figure 4-13 Connection State Diagram: Sink



4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using *USB PD* commands.

A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use *USB PD*.

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).

If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a *USB PD* PR_Swap.

If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.

If the port has entered the Attached.SNK state from the Attached.SRC state following a *USB PD* PR_Swap, the port shall terminate the connected CC pin to ground through Rd.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16

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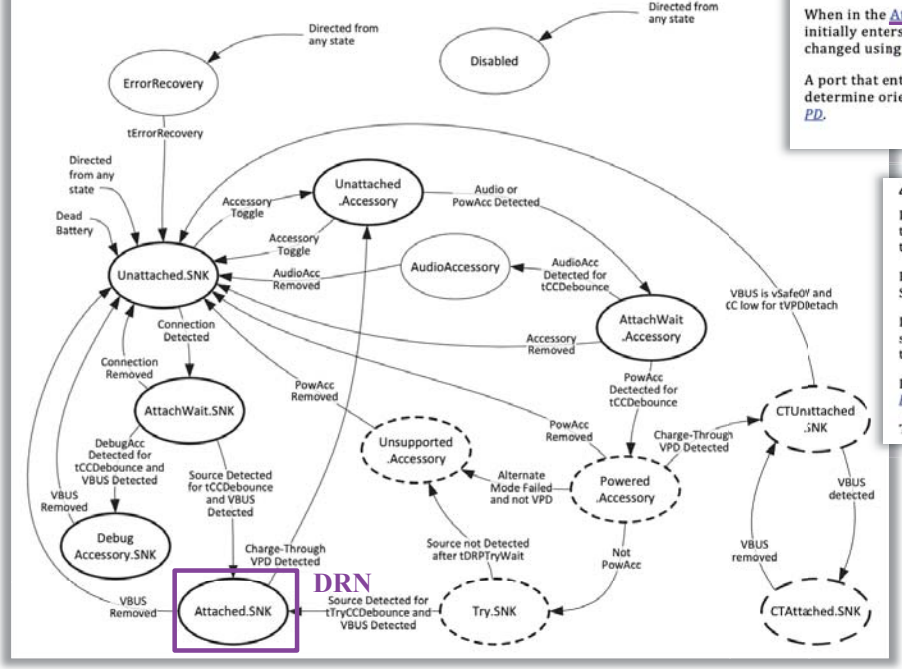
enabling operation of components of a **(PRO) processor system** to establish a **(DRN) state of power drain** thereof;

Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

Figure 4-14 Connection State Diagram: Sink with Accessory Support

PRO



4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using *USB PD* commands.

A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use *USB PD*.

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).

If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a *USB PD* PR_Swap.

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The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16

Exhibit H - U.S. Patent No. 8,477,514 – Samsung S2MM101

providing a **(S) signal to identify operation** of said **(PRO) processor system** in said **(DRN) state of power drain**;

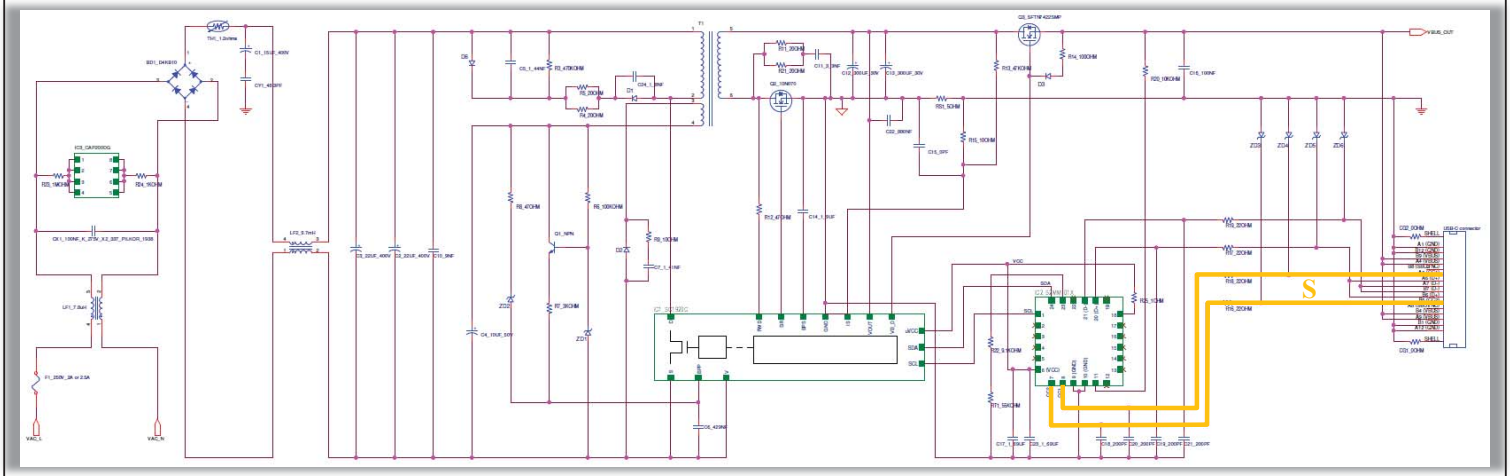

Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel S	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the USB 2.0 differential pair – Position 1	Second	B7	Dn2	Negative half of the USB 2.0 differential pair – Position 2	Second
A7	Dn1	Negative half of the USB 2.0 differential pair – Position 1	Second	B6	Dp2	Positive half of the USB 2.0 differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel S	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

S

Table 4-10 Source Perspective

CC1	CC2	State	Position
Open	Open	Nothing attached	N/A
Rd	Open	Sink attached DRN	①
Open	Rd		②
Open	Ra	Powered cable without Sink attached	①
Ra	Open		②
Rd	Ra	Powered cable with Sink, VCONN-Powered Accessory (VPA), or VCONN-Powered USB Device (VPD) attached	①
Ra	Rd		②
Rd	Rd	Debug Accessory Mode attached (Appendix B)	N/A
Ra	Ra	Audio Adapter Accessory Mode attached (Appendix A)	N/A

Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled. S
2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN. DRN
5. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16

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providing a **(S) signal to identify operation** of said **(PRO) processor system** in said **(DRN) state of power drain**;

PRO

4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

S

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.

Table 4-14 Source Port CC Pin State

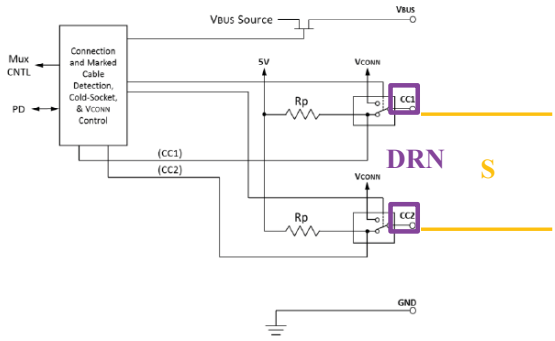
CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	Open, Rp	Above vOPEN
SRC.Rd	Rd	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	Ra	Below maximum vRa

Table 4-15 Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	Rp	Above minimum vRd-Connect
SNK.Open	Open, Ra, Rd	Below maximum vRa

Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.

Figure 4-7 Source Functional Model for CC1 and CC2



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1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
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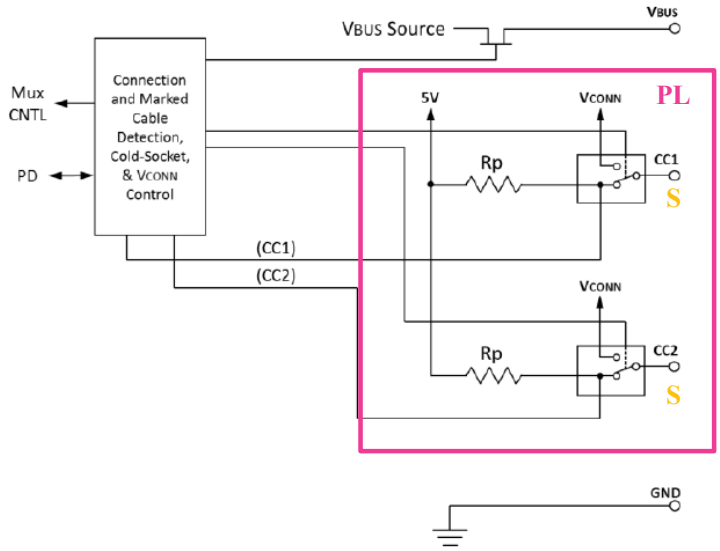
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN.
5. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

The source functional model detects CC1/CC2 and dynamically adjusts the current, voltage x current is the state of power drain.

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

sensing a **(PL) power level of said state of power drain** in response to said **(S) signal**; and

Figure 4-7 Source Functional Model for CC1 and CC2



The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16

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sensing a **(PL) power level of said state of power drain** in response to said **(S) signal**; and

Table 2-1 Summary of power supply options

Mode of Operation	Voltage	Current	Notes
USB 2.0	5 V	See USB 2.0	
USB 3.2	5 V	See USB 3.2	
USB4	5 V	1.5 A	See Section 5.3.
USB BC 1.2	5 V	1.5 A[1]	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 20 V	Configurable up to 5 A	Directional control and power level management

Figure 4-36 illustrates how the USB PD BMC signaling is carried over the USB Type-C cable's CC wire.

Figure 4-36 USB PD over CC Pins

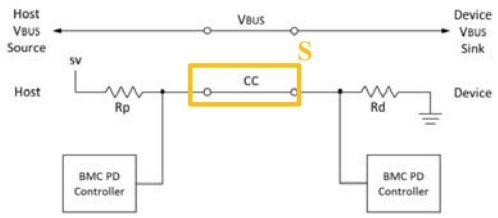


Table 4-11 Source (Host) and Sink (Device) Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Sink attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• Sense CC pins for orientation • Sense loss of VBUS for detach
Powered cable without Sink attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Powered cable with Sink, VCONN-Powered Accessory, or VCONN-Powered USB Device attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN • Detect VPD and remove VBUS	• If accessories or VPDs are supported, see Source Behavior with exception that VBUS is not applied., otherwise, N/A.
Debug Accessory Mode attached	• Sense CC pins for detach • Reconfigure for debug	• Sense VBUS for detach • Reconfigure for debug
Audio Adapter Accessory Mode attached	• Sense CC pins for detach • Reconfigure for analog audio	• If accessories are supported, see Source Behavior, otherwise, N/A

Table 4-17 Precedence of power source usage

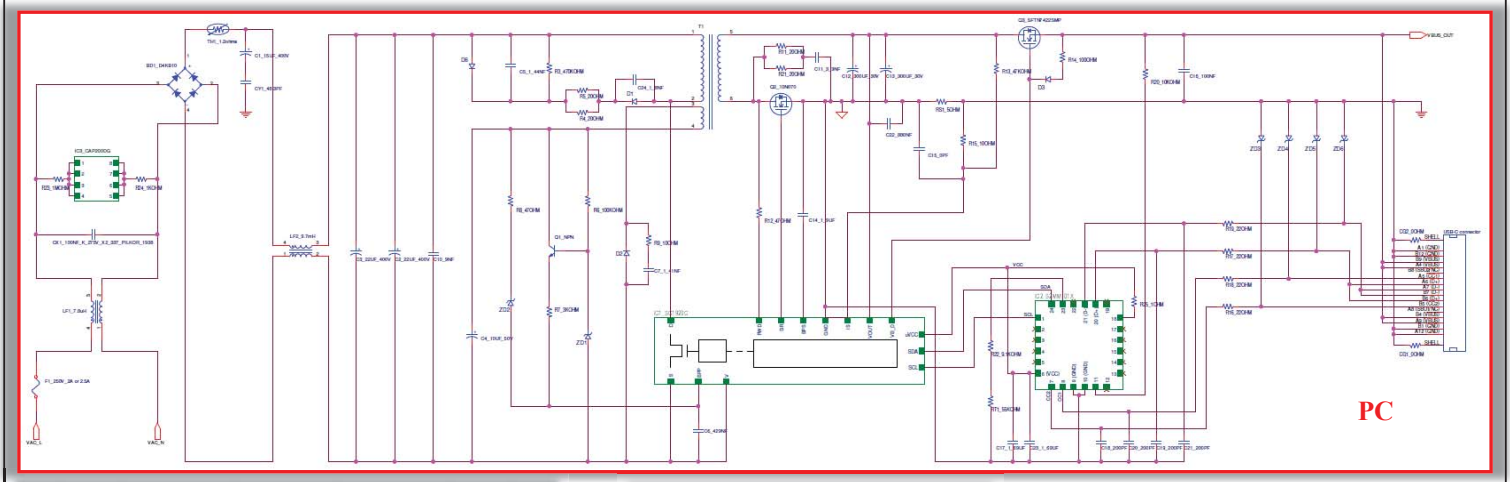
Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	USB PD		Configurable	5 A
↓	USB Type-C Current @ 3.0 A		5 V	3.0 A
	USB Type-C Current @ 1.5 A		5 V	1.5 A
	USB BC 1.2		5 V	Up to 1.5 A[1]
Lowest	Default USB Power	USB 3.2	5 V	See USB 3.2
		USB 2.0	5 V	See USB 2.0

Source: Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019; Note: The citation pertains to only the document excerpt not the schematics or other data.

Claim 16

Exhibit H - U.S. Patent No. 8,477,514 – Samsung S2MM101

controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.



Claim 16

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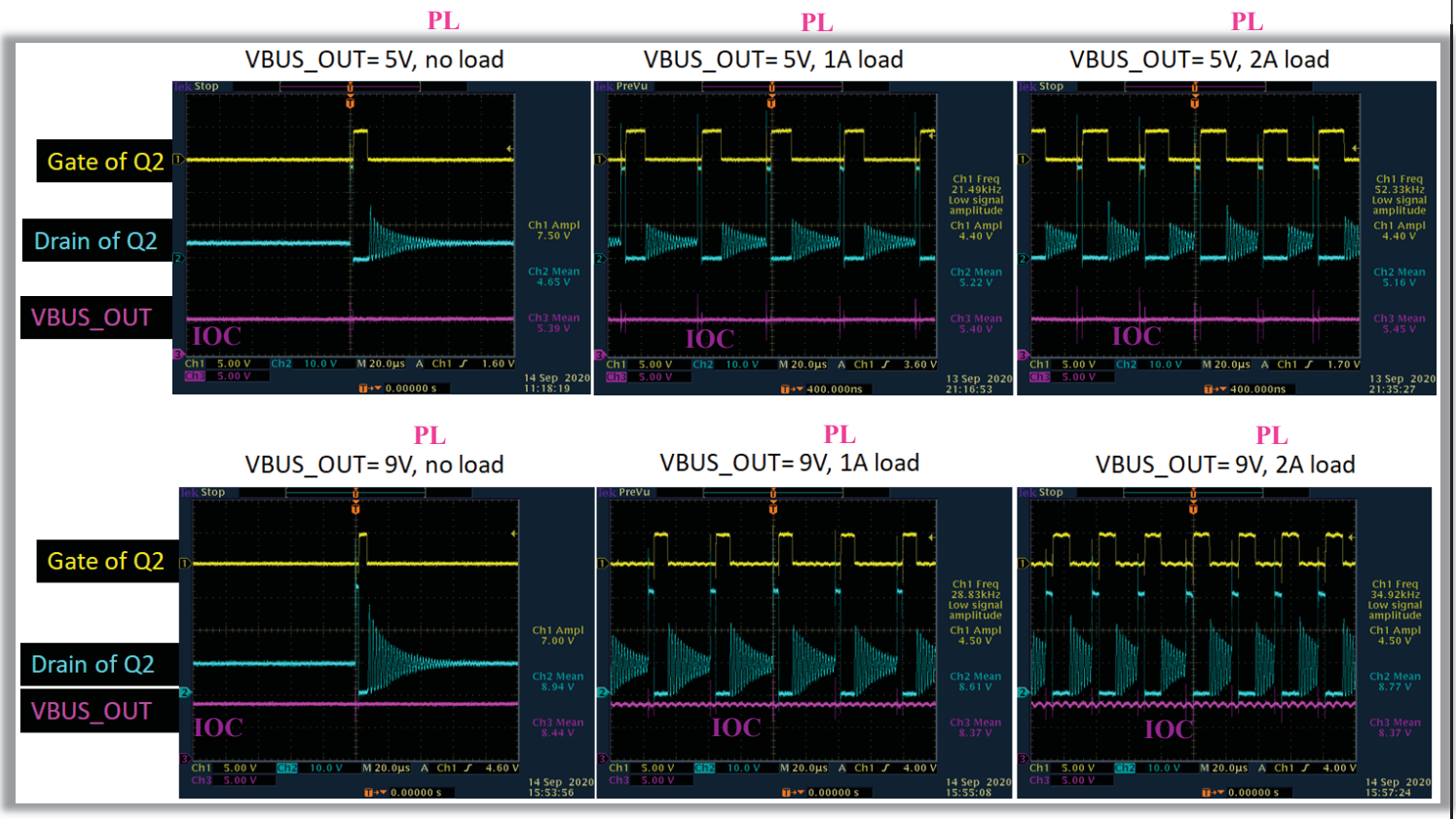
controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.



Claim 16

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controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.